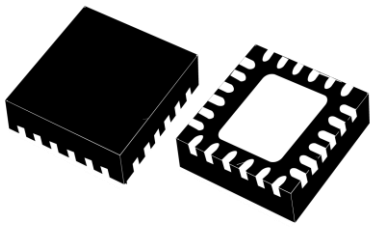
LNBH25LS

LNB supply and control IC with step-up and I²C interface

Datasheet - production data



QFN24 (4x4 mm)

Features

- Complete interface between LNB and I²C bus
- Built-in DC-DC converter for single 12 V supply operation and high efficiency (typ. 93% @ 0.5 A)
- Selectable output current limit by external resistor
- Compliant with main satellite receiver output voltage specifications (15 programmable levels)
- Accurate built-in 22 kHz tone generator suits widely accepted standards
- 22 kHz tone waveform integrity guaranteed at no-load condition
- Low drop post regulator and high efficiency step-up PWM with integrated power NMOS allowing low power losses
- Overload and overtemperature internal protections with I²C diagnostic bits
- LNB short-circuit dynamic protection
- +/- 4 kV ESD tolerant on output power pins

Applications

- STB satellite receivers
- TV satellite receivers
- PC card satellite receivers

Description

Intended for analog and digital satellite receivers/Sat-TV and Sat-PC cards, the LNBH25LS is a monolithic voltage regulator and interface IC, assembled in QFN24L (4x4 mm) specifically designed to provide 13/18 V power supply and 22 kHz tone signaling to the LNB down-converter in the antenna dish or to the multi-switch box. In this application field, it offers a complete solution with extremely low component count and low power dissipation together with a simple design and I²C standard interface.

Table 1: Device summary

Order code	Package	Packing
LNBH25LSPQR	QFN24L (4x4 mm)	Tape and reel

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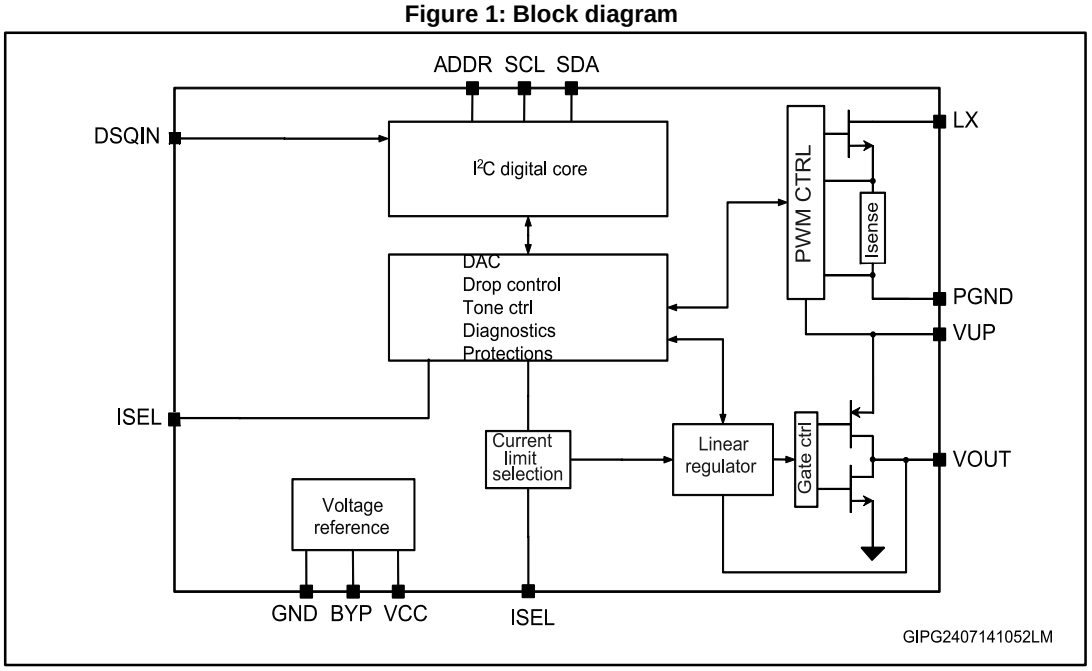
1 Block diagram

Figure 1: Block diagram



2 Application information

This IC has a built-in DC-DC step-up converter that, from a single source (8 V to 16 V), generates the voltages (V_{up}) that let the integrated LDO post-regulator (generating the 13 V /18 V LNB output voltages plus the 22 kHz DiSEqC™ tone) work with a minimum dissipated power of 0.5 W typ. @ 500 mA load (the LDO drop voltage is internally kept at V_{UP}-V_{OUT} = 1 V typ.). The IC is also provided with an undervoltage lockout circuit that disables the whole circuit when the supplied V_{CC} drops below a fixed threshold (4.7 V typ.). The step-up converter soft-start function reduces the inrush current during startup. The SS time is internally fixed at 4 ms typ. to switch from 0 to 13 V and 6 ms typ. to switch from 0 to 18 V.

2.1 DiSEqC data encoding (DSQIN pin)

The internal 22 kHz tone generator is factory trimmed in accordance to DiSEqC standards, and can be activated in 3 different ways:

1. By an external 22 kHz source DiSEqC data connected to the DSQIN logic pin (TTL compatible). In this case the I²C tone control bits must be set: EXTM = TEN = 1
2. By an external DiSEqC data envelope source connected to the DSQIN logic pin. In this case the I²C tone control bits must be set: EXTM = 0 and TEN = 1
3. Through the TEN I²C bit if a 22 kHz presence is requested in continuous mode. In this case the DSQIN TTL pin must be pulled HIGH and EXTM bit set to “0”

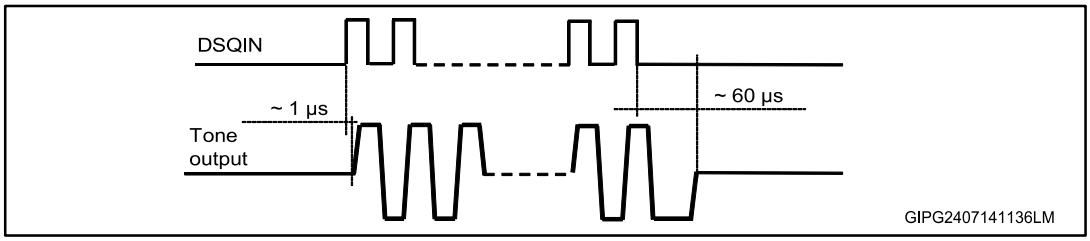
2.2 Data encoding by external 22 kHz tone TTL signal

In order to improve design flexibility an external tone signal can be input to the DSQIN pin by setting the EXTM bit to “1”.

The DSQIN is a logic input pin which activates the 22 kHz tone to the VOUT pin, by using the LNBH25LS integrated tone generator.

The output tone waveforms are internally controlled by the LNBH25LS tone generator in terms of rise/fall time and tone amplitude, while, the external 22 kHz signal on the DSQIN pin is used to define the frequency and the duty cycle of the output tone. A TTL compatible 22 kHz signal is required for the proper control of the DSQIN pin function. Before sending the TTL signal on the DSQIN pin, the EXTM and TEN bits must be previously set to “1”. As soon as the DSQIN internal circuit detects the 22 kHz TTL external signal code, the LNBH25LS activates the 22 kHz tone on the V_{OUT} output with about 1 µs delay from TTL signal activation, and it stops with about 60 µs delay after the 22 kHz TTL signal on DSQIN has expired, refer to *Figure 2: "Tone enable and disable timing (using external waveform)"*.

Figure 2: Tone enable and disable timing (using external waveform)

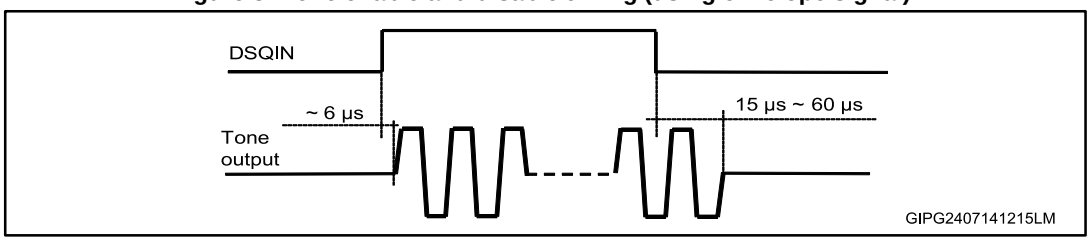


2.3 Data encoding by external DiSEqC envelope control through the DSQIN pin

If an external DiSEqC envelope source is available, it is possible to use the internal 22 kHz generator activated during the tone transmission by connecting the DiSEqC envelope source to the DSQIN pin. In this case the I²C tone control bits must be set: EXTM = 0 and TEN = 1. In this way, the internal 22 kHz signal is superimposed to the V_{OUT} DC voltage to generate the LNB output 22 kHz tone. During the period in which the DSQIN is kept HIGH, the internal control circuit activates the 22 kHz tone output.

The 22 kHz tone on the VOUT pin actives with about 6 µs delay from the DSQIN TTL signal rising edge, and it stops with a delay time in the range from 15 µs to 60 µs after the 22 kHz TTL signal on DSQIN has expired, refer to *Figure 3: "Tone enable and disable timing (using envelope signal)"*.

Figure 3: Tone enable and disable timing (using envelope signal)



2.4 Output current limit selection

The linear regulator current limit threshold can be set by an external resistor connected to the ISEL pin. The resistor value defines the output current limit by the equation:

$$I_{LIM}(typ.) = \frac{13915}{RSEL^{1.111}}$$

GIPG2507140950LM

where RSEL is the resistor connected between ISEL and GND expressed in kΩ and I_{LIM}(typ.) is the typical current limit threshold expressed in mA. I_{LIM} can be set up to 750 mA.

2.5 Output voltage selection

The linear regulator output voltage level can be easily programmed in order to accomplish application specific requirements, using 4 bits of an internal data 1 register, see *Section 7.3: "Data registers"* and *Table 13: "Output voltage selection table (data1 register, write mode)"* for exact programmable values. Register writing is accessible via the I²C bus.

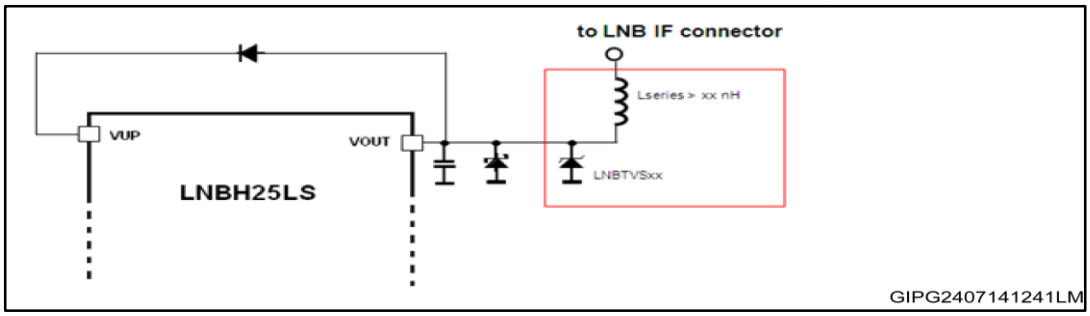
2.6 Diagnostic and protection functions

The LNBH25LS has 3 diagnostic internal functions provided by I²C bus, by reading 3 bits on the status 1 register (in read mode). All the diagnostic bits are, in normal operation (that is no failure detected), set to LOW. Two diagnostic bits are dedicated to the overtemperature and overload protection status (OTF and OLF). One bit is dedicated to the input voltage (PNG) function. Once OLF (or OTF or PNG) bit has been activated (set to “1”), it is latched to “1” until relevant cause is removed and a new register reading operation is done.

2.7 Surge protections and TVS diodes

The LNBH25LS device is directly connected to the antenna cable in a set-top box. Atmospheric phenomenon can cause high voltage discharges on the antenna cable causing damage to the attached devices. Surge pulses occur due to direct or indirect lightning strikes to an external (outdoor) circuit. This leads to currents or electromagnetic fields causing high voltage or current transients. Transient voltage suppressor (TVS) devices are usually placed, as shown in the following schematic, to protect the STB output circuits where the LNBH25LS and other devices are electrically connected to the antenna cable.

Figure 4: Surge protection circuit



For this purpose we recommend the use of LNBTVSxx surge protection diodes specifically designed by ST. The selection of LNBTVS diodes should be based on the maximum peak power dissipation supported by the diode, see the LNBTVS datasheet for further details.

2.8 Power-on I²C interface reset and undervoltage lockout

The I²C interface built into the LNBH25LS is automatically reset at power-on. As long as the V_{CC} stays below the undervoltage lockout (UVLO) threshold (4.7 V typ.), the interface does not respond to any I²C command and all data register bits are initialized to zeros, therefore keeping the power blocks disabled. Once the V_{CC} rises above 4.8 V typ. the I²C interface becomes operative and the data registers can be configured by the main microprocessor.

2.9 PNG: input voltage minimum detection

When input voltage (VCC pin) is lower than LPD (low power diagnostic) minimum thresholds, the PNG I²C bit is set to “1”.

2.10 COMP: boost capacitors and inductor

The DC-DC converter compensation loop can be optimized in order to properly work with both ceramic and electrolytic capacitors (VUP pin). For this purpose, one I²C bit in the data 4 register, see COMP *Table 9: "Data 4 (read/write register. Register address = 0X5)"* can be set to “1” or “0” as follows:

- COMP = 0 for electrolytic capacitors
- COMP = 1 for ceramic capacitors

For recommended DC-DC capacitor and inductor values refer to *Section 5: "Typical application circuits"* and to the BOM in *Table 5: "DiSEqC 1.x bill of material"*.

2.11 OLF: overcurrent, short-circuit protection and diagnostic

In order to reduce the total power dissipation during an overload or a short-circuit condition, the device is provided with a dynamic short-circuit protection. It is possible to set short-

circuit current protection either statically (simple current clamp) or dynamically by the PCL bit of the I²C data 3 register. When the PCL (pulsed current limiting) bit LOW, the overcurrent protection circuit works dynamically: as soon as an overload is detected, the output current is provided for T_{ON} time 90 ms, after which the output is set in shutdown for T_{OFF} time of typically 900 ms. Simultaneously, the diagnostic OLF I²C bit of the system register is set to “1”. After this time has elapsed, the output is resumed for a time T_{ON}. At the end of T_{ON}, if the overload is still detected, the protection circuit cycles again through T_{OFF} and T_{ON}. At the end of a full T_{ON} in which no overload is detected, normal operation is resumed and the OLF diagnostic bit is reset to LOW after a register reading is done. Typical T_{ON} +T_{OFF} time is 990 ms and an internal timer determines it. This dynamic operation can greatly reduce the power dissipation in short-circuit condition, still ensuring excellent power-on startup in most conditions. However, there could be some cases in which a highly capacitive load on the output may cause a difficult startup when the dynamic protection is chosen. This can be solved by initiating any power startup in static mode (PCL=1) and, then, switching to the dynamic mode (PCL=0) after a chosen amount of time depending on the output capacitance. Also in static mode, the diagnostic OLF bit goes to “1” when the current clamp limit is reached and returns LOW when the overload condition is cleared and register reading is done.

After the overload condition is removed, normal operation can be resumed in two ways, according to the OLR I²C bit on the data 4 register.

If OLR=1, all VSEL 1..4 bits are reset to “0” and LNB output (VOUT pin) is disabled. To re-enable output stage, the VSEL bits must be set again by the microprocessor, and the OLF bit is reset to “0” after a register reading operation.

If OLR=0, output is automatically re-enabled as soon as the overload condition is removed, and the OLF bit is reset to “0” after a register reading operation.

2.12 OTF: thermal protection and diagnostic

The LNBH25LS is also protected against overheating: when the junction temperature exceeds 150 °C (typ.), the step-up converter and the linear regulator are shut off, the diagnostic OTF bit in the status1 register is set to “1”. After the overtemperature condition is removed, normal operation can be resumed in two ways, according to the THERM I²C bit on the data 4 register.

If THERM=1, all VSEL 1..4 bits are reset to “0” and LNB output (VOUT pin) is disabled. To re-enable output stage, the VSEL bits must be set again by the microprocessor, while the OTF bit is reset to “0” after a register reading operation.

If THERM=0, output is automatically re-enabled as soon as the overtemperature condition is removed, while the OTF bit is reset to “0” after a register reading operation.

3 Pin configuration

Figure 5: Pin connections (top view)

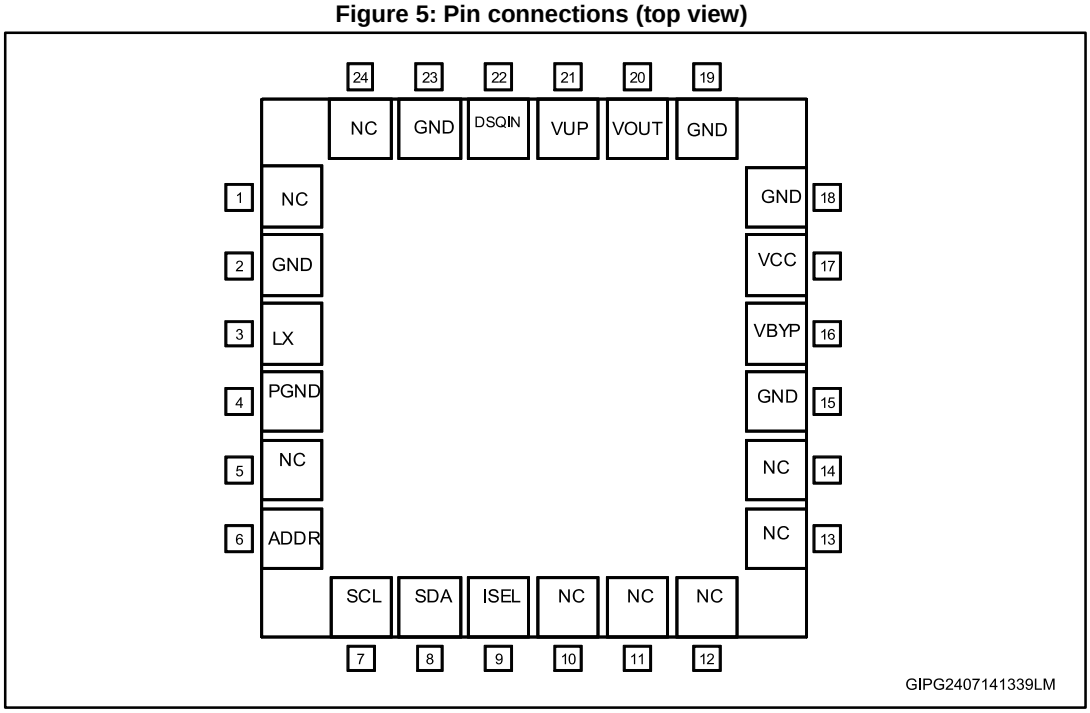


Table 2: Pin description

Pin	Symbol	Name	Function
3	LX	NMOS drain	Integrated N-channel Power MOSFET drain
4	PGND	Power ground	DC-DC converter power ground. To be connected directly to the exposed pad
6	ADDR	Address setting	Two I²C bus addresses available by setting the address pin level voltage. See *Table 15: "Address pin characteristics"*
7	SCL	Serial clock	Clock from I²C BUS
8	SDA	Serial data	Bi-directional data from/to I²C bus
9	ISEL	Current selection	The resistor “RSEL” connected between ISEL and GND defines the linear regulator current limit threshold. See *Section 6.5: "Transmission without acknowledge"*
2,15,18, 19,23	GND	Analog ground	Analog circuits ground. To be connected directly to the exposed pad
16	VBYP	Bypass capacitor	Needed for internal pre-regulator filtering. The VBYP pin is intended only to connect an external ceramic capacitor. Any connection of this pin to external current or voltage sources may cause permanent damage to the device
17	VCC	Supply input	8 to 16 V IC DC-DC power supply
20	VOUT	LNB output port	Output of the integrated very low drop linear regulator. See *Table 13: "Output voltage selection table (data1 register, write mode)"* for voltage selections and description

Pin	Symbol	Name	Function
21	VUP	Step-up voltage	Input of the linear post-regulator. The voltage on this pin is monitored by the internal step-up controller to keep a minimum dropout across the linear pass transistor
22	DSQIN	DSQIN for DiSEqC envelope input or external 22 kHz TTL input	It can be used as DiSEqC envelope input or external 22 kHz TTL input depending on the EXTM I²C bit setting as follows: EXTM=0, TEN=1: it accepts the DiSEqC envelope code from the main microcontroller. The LNBH25LS uses this code to modulate the internally generated 22 kHz carrier. If EXTM=TEN=1: it accepts external 22 kHz logic signals which activate the 22 kHz tone output, refer to *Section 2.3: "Data encoding by external DiSEqC envelope control through the DSQIN pin"*. Pull-up high if the tone output is activated only by the TEN I²C bit
Epad	Epad	Exposed pad	To be connected with power grounds and to the ground layer through vias to dissipate the heat
1, 5, 10, 11, 12, 13, 14, 24	NC	Not internally connected	Not internally connected pins. These pins can be connected to GND to improve thermal performance

4 Maximum ratings

Table 3: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC power supply input voltage pins	-0.3 to 20	V
V_{UP}	DC input voltage	-0.3 to 40	V
I_{OUT}	Output current	Internally limited	mA
V_{OUT}	DC output pin voltage	-0.3 to 40	V
V_I	Logic input pin voltage (SDA, SCL, DSQIN, ADDR pins)	-0.3 to 7	V
LX	LX input voltage	-0.3 to 30	V
V_{BYP}	Internal reference pin voltage	-0.3 to 4.6	V
ISEL	Current selection pin voltage	-0.3 to 3.5	V
T_{STG}	Storage temperature range	-50 to 150	°C
T_J	Operating junction temperature range	-25 to 125	°C
ESD	ESD rating with human body model (HBM) all pins, unless power output pins	2	kV
	ESD rating with human body model (HBM) for power output pins	4	

Table 4: Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case	2	°C/W
R_{thJA}	Thermal resistance junction-ambient with device soldered on 2s2p 4-layer PCB provided with thermal vias below exposed pad	40	°C/W

Absolute maximum ratings are those values beyond which damage to the device may occur. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to network ground terminal.

5 Typical application circuits

Figure 6: DiSEqC 1.x application circuit

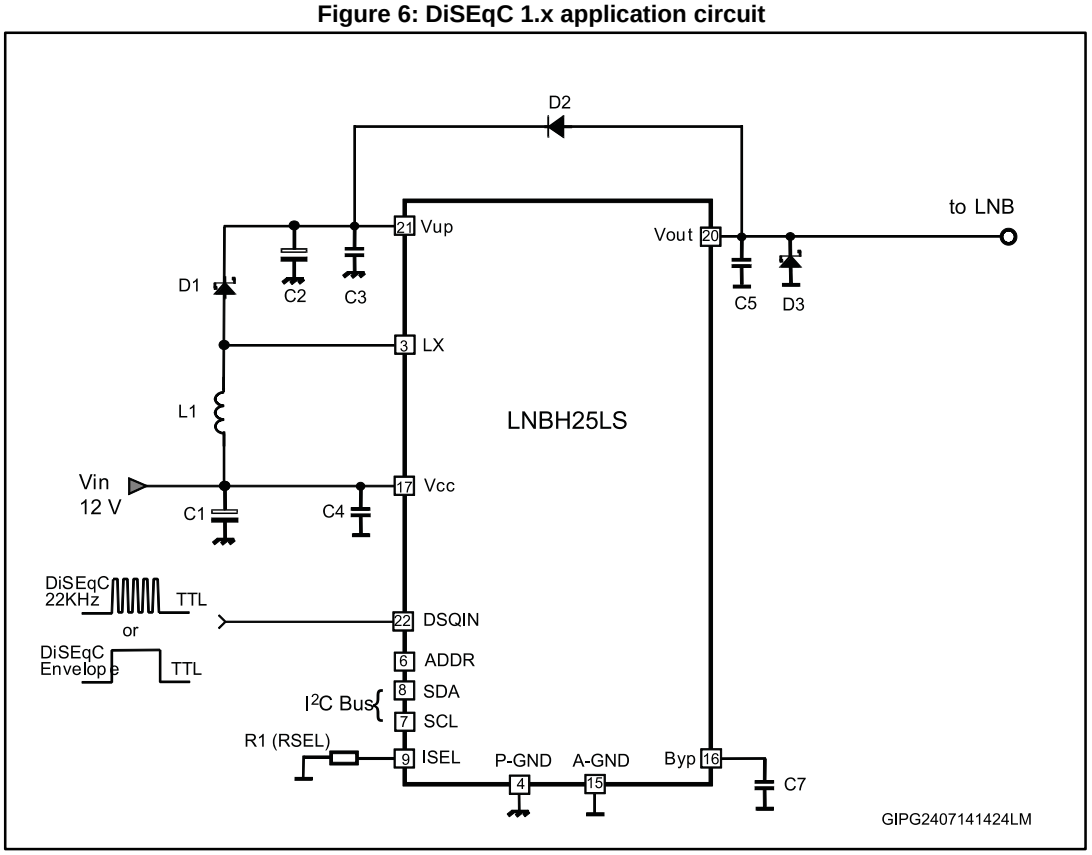


Table 5: DiSEqC 1.x bill of material

Component	Notes
R1 (RSEL)	SMD resistor. Refer to *Table 12: "Electrical characteristics"* and ISEL pin description in *Table 2: "Pin description"*
C1	> 25 V electrolytic capacitor, 100 µF or higher is suitable or > 25 V ceramic capacitor, 10 µF or higher is suitable
C2	With COMP = 0, > 25 V electrolytic capacitor, 100 µF or higher is suitable or with COMP = 1, > 35 V ceramic capacitor, 22 µF (or 2 x 10 µF) or higher is suitable
C3	From 470 nF to 2.2 µF ceramic capacitor placed as close as possible to V_{UP} pins. Higher values allow lower DC-DC noise
C5	From 100 nF to 220 nF ceramic capacitor placed as close as possible to V_{OUT} pins. Higher values allow lower DC-DC noise
C4, C7	220 nF ceramic capacitors. To be placed as close as possible to VOUT pin
D1	STPS130A or similar Schottky diode
D2	1N4001-07, S1A-S1M, or any similar general purpose rectifier

Component	Notes
D3	BAT54, BAT43, 1N5818, or any low power Schottky diode with $I_F(AV) > 0.2$ A, $V_{RRM} > 25$ V, $V_F < 0.5$ V. To be placed as close as possible to VOUT pin
L1	With COMP=0, use 10 µH inductor with $I_{SAT} > I_{PEAK}$ where I_{PEAK} is the boost converter peak current or with COMP=1 and C2 = 22 µF, use 6.8 µH inductor with $I_{SAT} > I_{PEAK}$ where I_{PEAK} is the boost converter peak current

6 I²C bus interface

Data transmission from the main microprocessor to the LNBH25LS and vice versa takes place through the 2-wire I²C bus interface, consisting of the 2-line SDA and SCL (pull-up resistors to positive supply voltage must be externally connected).

6.1 Data validity

As shown in *Figure 7: "Data validity on the I²C bus"*, the data on the SDA line must be stable during the high semi-period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

6.2 Start and stop condition

As shown in *Figure 8: "Timing diagram of I²C bus"*, a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH. A stop condition must be sent before each start condition.

6.3 Byte format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

6.4 Acknowledge

The master (microprocessor) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse, see *Figure 9: "Acknowledge on the I²C bus"*. The peripheral (LNBH25LS), which acknowledges, must pull down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse. The peripheral, which has been addressed, has to generate acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the stop information in order to abort the transfer. The LNBH25LS doesn't generate acknowledge if V_{CC} supply is below the undervoltage lockout threshold (4.7 V typ.).

6.5 Transmission without acknowledge

Avoiding to detect acknowledges of the LNBH25LS, the microprocessor can use a simpler transmission: it simply waits for one clock without checking the slave acknowledging, and sends the new data. This approach is of course less protected from misworking and decreases noise immunity.

Figure 7: Data validity on the I²C bus

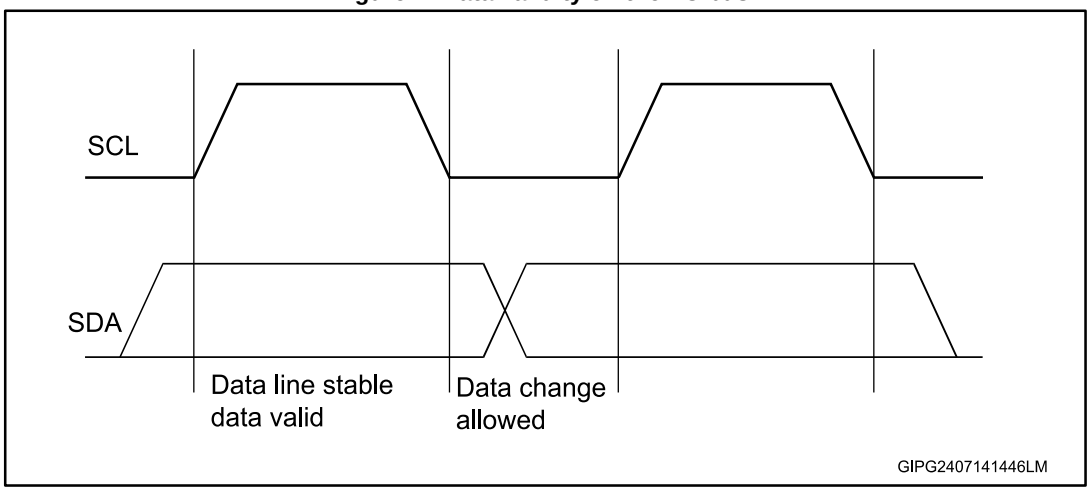


Figure 8: Timing diagram of I²C bus

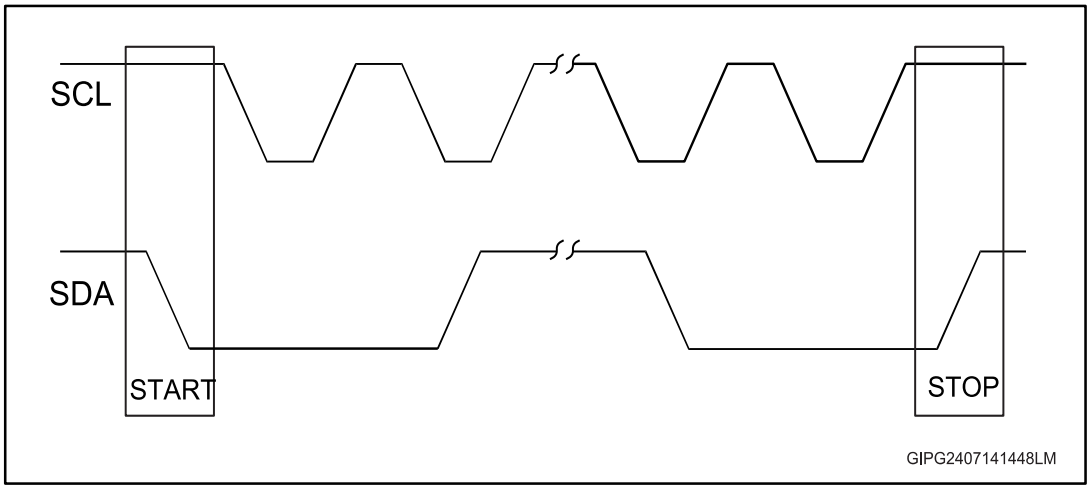
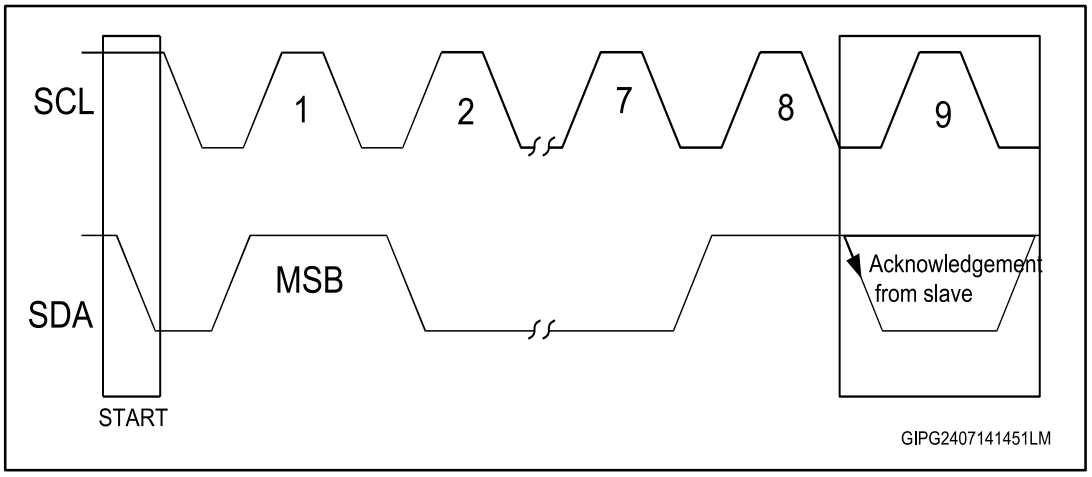


Figure 9: Acknowledge on the I²C bus



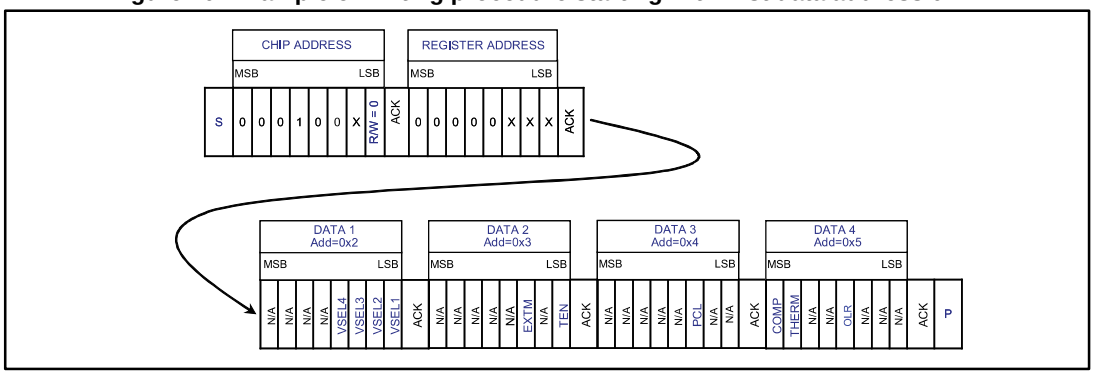
7 I²C interface protocol

7.1 Write mode transmission

The LNBH25S interface protocol is made up of:

- A start condition (S)
- A chip address byte with the LSB bit R/W = 0
- A register address (internal address of the first register to be accessed)
- A sequence of data (byte to write to the addressed internal register + acknowledge)
- The following bytes, if any, to be written to successive internal registers
- A stop condition (P). The transfer lasts until a stop bit is encountered
- The LNBH25S, as slave, acknowledges every byte transfer

Figure 10: Example of writing procedure starting with first data address 0X2



ACK = acknowledge

S = start

P = stop

R/W = 1/0, read/write bit

X = 0/1, set the values to select the chip address.

The writing procedure can start from any register address by simply setting X values in the register address byte (after the chip address). It can be also stopped by the master by sending a stop condition after any acknowledge bit.

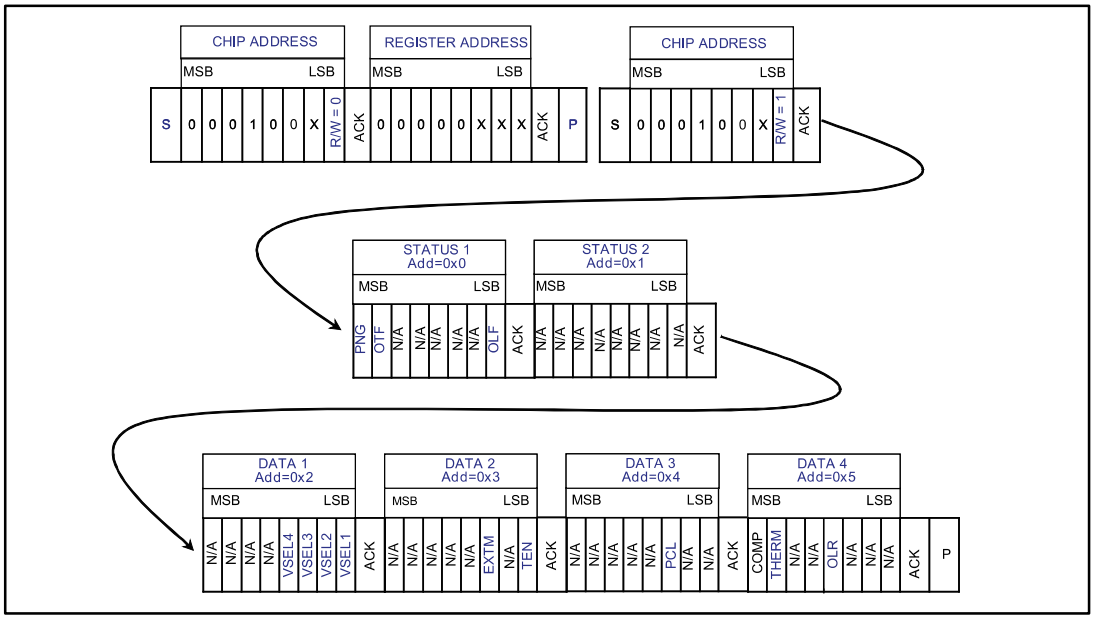
7.2 Read mode transmission

In read mode the byte sequence as follows:

- A start condition (S)
- A chip address byte with the LSB bit R/W=0
- The register address byte of the internal first register to be accessed
- A stop condition (P)
- A new master transmission with the chip address byte and the LSB bit R/W=1
- After acknowledge, the LNBH25S starts to send the addressed register content. As long as the master keeps the acknowledge low, the LNBH25S transmits the next address register byte content

- The transmission is terminated when the master sets the acknowledge high with the following stop bit

Figure 11: Example of reading procedure starting with first status address 0X0



ACK = acknowledge

S = start

P = stop

R/W = 1/0, read/write bit

X = 0/1, set the values to select the chip address.

The writing procedure can start from any register address (status 1, 2 or data 1..4) by simply setting X values in the register address byte (after the chip address). It can be also stopped by the master by sending a stop condition after any acknowledge bit.

7.3 Data registers

The data 1..4 registers can be addressed both in write and read mode. In read mode they return the last writing byte status received in the previous write transmission.

The following tables provide the register address values of data 1..4 and a function description of each bit.

Table 6: Data 1 (read/write register. Register address = 0X2)

Bit	Name	Value	Description
Bit 0 (LSB)	VSEL1	0/1	Output voltage selection bits. See *Table 13: "Output voltage selection table (data1 register, write mode)"*
Bit 1	VSEL2	0/1	
Bit 2	VSEL3	0/1	
Bit 3	VSEL4	0/1	

Bit	Name	Value	Description
Bit 4	N/A	0	Reserved. Keep to “0”
Bit 5	N/A	0	Reserved. Keep to “0”
Bit 6	N/A	0	Reserved. Keep to “0”
Bit 7 (MSB)	N/A	0	Reserved. Keep to “0”

N/A = reserved bit

All bits reset to “0” at power-on

Table 7: Data 2 (read/write register. Register address = 0X3)

Bit	Name	Value	Description
Bit 0 (LSB)	TEN	1	22 kHz tone enabled. Tone output controlled by DSQIN pin
		0	22 kHz tone output disabled
Bit 1	N/A	0	Reserved. Keep to “0”
Bit 2	EXTM	1	DSQIN input pin is set to receive external 22 kHz TTL signal source
		0	DSQIN input pin is set to receive external DiSEqC envelope TTL signal
Bit 3	N/A	0	Reserved. Keep to “0”
Bit 4	N/A	0	Reserved. Keep to “0”
Bit 5	N/A	0	Reserved. Keep to “0”
Bit 6	N/A	0	Reserved. Keep to “0”
Bit 7 (MSB)	N/A	0	Reserved. Keep to “0”

N/A = reserved bit

All bits reset to 0 at power-on

Table 8: Data 3 (read/write register. Register address = 0X4)

Bit	Name	Value	Description
Bit 0 (LSB)	N/A	1	Reserved. Keep to “0”
Bit 1	N/A	0	Reserved. Keep to “0”
Bit 2	PCL	1	Pulsed (dynamic) LNB output current limiting is deactivated
		0	Pulsed (dynamic) LNB output current limiting is activated
Bit 3	N/A	0	Reserved. Keep to “0”
Bit 4	N/A	0	Reserved. Keep to “0”
Bit 5	N/A	0	Reserved. Keep to “0”
Bit 6	N/A	0	Reserved. Keep to “0”
Bit 7 (MSB)	N/A	0	Reserved. Keep to “0”

N/A = reserved bit

All bits reset to 0 at power-on

Table 9: Data 4 (read/write register. Register address = 0X5)

Bit	Name	Value	Description
Bit 0 (LSB)	N/A	0	Reserved. Keep to “0”
Bit 1	N/A	0	Reserved. Keep to “0”
Bit 2	N/A	0	Reserved. Keep to “0”
Bit 3	OLR	1	In case overload protection activation (OLF=1), all VSEL 1..4 bits are reset to “0” and LNB output (VOUT pin) is disabled. The VSEL bit must be set again by the master after the overcurrent condition is removed (OLF=0)
		0	In case of overload protection activation (OLF=1) the LNB output (VOUT pin) is automatically enabled as soon as the overload condition is removed (OLF=0) with the previous VSEL bits setting
Bit 4	N/A	0	Reserved. Keep to “0”
Bit 5	N/A	0	Reserved. Keep to “0”
Bit 6	THERM	1	If thermal protection is activated (OTF=1), all VSEL 1..4 bits are reset to “0” and LNB output (VOUT pin) is disabled. The VSEL bit must be set again by the master after the overtemperature condition is removed (OTF=0)
		0	In case of thermal protection activation (OTF=1) the LNB output (VOUT pin) is automatically enabled as soon as the overtemperature condition is removed (OTF=0) with the previous VSEL bits setting
Bit 7 (MSB)	COMP	1	DC-DC converter compensation: set to use very low E.S.R. capacitors or ceramic caps on VUP pin
		0	DC-DC converter compensation: set to use standard electrolytic capacitors on VUP pin

N/A = reserved bit

All bits reset to 0 at power-on

7.4 Status registers

The status 1, 2 registers can be addressed only in read mode and provide the diagnostic functions described in the following tables.

Table 10: Status 1 (read register. Register address = 0X0)

Bit	Name	Value	Description
Bit 0 (LSB)	OLF	1	VOUT pin overload protection has been triggered (I_{OUT} > I_{LIM}). Refer to *Table 8: "Data 3 (read/write register. Register address = 0X4)"* for the overload operation settings (PCL bit)
		0	No overload protection has been triggered to the VOUT pin (I_{OUT} < I_{LIM})
Bit 1	N/A	-	Reserved
Bit 2	N/A	-	Reserved
Bit 3	N/A	-	Reserved
Bit 4	N/A	-	Reserved
Bit 5	N/A	-	Reserved
Bit 6	OTF	1	Junction overtemperature is detected, T_J > 150 °C. See also THERM bit setting in *Table 9: "Data 4 (read/write register. Register address = 0X5)"*
		0	Junction overtemperature not detected, T_J < 135 °C. T_J is below thermal protection threshold
Bit 7 (MSB)	PNG	1	Input voltage (VCC pin) lower than LPD minimum thresholds. Refer to *Table 12: "Electrical characteristics"*
		0	Input voltage (VCC pin) higher than LPD thresholds. Refer to *Table 12: "Electrical characteristics"*

N/A = reserved bit

All bits reset to 0 at power-on

Table 11: Status 2 (read register. Register address = 0X1)

Bit	Name	Value	Description
Bit 0 (LSB)	N/A	-	Reserved
Bit 1	N/A	-	Reserved
Bit 2	N/A	-	Reserved
Bit 3	N/A	-	Reserved
Bit 4	N/A	-	Reserved
Bit 5	N/A	-	Reserved
Bit 6	N/A	-	Reserved
Bit 7 (MSB)	N/A	-	Reserved

N/A = reserved bit

All bits reset to 0 at power-on

8 Electrical characteristics

Refer to *Section 5: "Typical application circuits"*, T_J from 0 to 85 °C, all data 1..4 register bits set to 0 unless VSEL1 = 1, RSEL = 16.2 kΩ, DSQIN = LOW, V_{IN} = 12 V, I_{OUT} = 50 mA, unless otherwise stated. Typical values are referred to T_J = 25 °C. V_{OUT} = VOUT pin voltage. See software description section for I²C access to the system register *Section 6: "I²C bus interface"*.

Table 12: Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Supply voltage (1)		8	12	16	V
I_{IN}	Supply current	I_{OUT} = 0 mA		6		mA
		22 kHz tone enabled (TEN=1), DSQIN = high, I_{OUT}= 0 mA		10		mA
		VSEL1=VSEL2= VSEL3=VSEL4=0		1		mA
V_{OUT}	Output voltage total accuracy	Valid at any V_{OUT} selected level	-3.5		+3.5	%
V_{OUT}	Line regulation	V_{IN} = 8 to 16 V			40	mV
V_{OUT}	Load regulation	I_{OUT} from 50 to 750 mA		75	100	
I_{LIM}	Output current limiting thresholds	RSEL = 16.2 kΩ	500		750	mA
		RSEL = 22 kΩ	350		550	
I_{SC}	Output short-circuit current	RSEL = 16.2 kΩ		350		mA
SS	Soft-start time	V_{OUT} from 0 to 13 V		4		ms
SS	Soft-start time	V_{OUT} from 0 to 18 V		6		ms
T13-18	Soft transition rise time	V_{OUT} from 13 to 18 V		1.5		ms
T18-13	Soft transition fall time	V_{OUT} from 18 to 13 V		1.5		ms
T_{OFF}	Dynamic overload protection OFF time	PCL=0, output shorted		900		msV$_{PP}$
T_{ON}	Dynamic overload protection ON time	PCL = 0, output shorted		T_{OFF}/10		
A_{TONE}	Tone amplitude	DSQIN=high, EXTM=0, TEN=1 I_{OUT} from 0 to 750 mA C_{BUS} from 0 to 750 nF	0.55	0.675	0.8	
F_{TONE}	Tone frequency	DSQIN=high, EXTM=0, TEN=1 I_{OUT} from 0 to 500 mA C_{BUS} from 0 to 750 nF	20	22	24	kHz
D_{TONE}	Tone duty cycle		43	50	57	%
tr, tf	Tone rise or fall time (2)		5	8	15	µs
$Eff_{DC/DC}$	DC-DC converter efficiency	I_{OUT} = 500 mA		93		%
F_{SW}	DC-DC converter switching frequency			440		kHz
UVLO	Undervoltage lockout thresholds	UVLO threshold rising		4.8		V
		UVLO threshold falling		4.7		
V_{LP}	Low power diagnostic	V_{LP} threshold rising		7.2		V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
	(LPD) thresholds	V_{LP} threshold falling		6.7		
V_{IL}	DSQIN, pin logic low				0.8	V
V_{IH}	DSQIN, pin logic high		2			V
I_{IH}	DSQIN, pin input current	V_{IH} = 5 V		15		µA
I_{OBK}	Output backward current	All VSELx=0, V_{OBK} = 30 V		-3	-6	mA
I_{SINK}	Output low-side sink current	V_{OUT} forced at V_{OUT_NOM} + 0.1 V		70		mA
$I_{SINK\_}$ TIME-OUT	Low-side sink current time-out	V_{OUT} forced at V_{OUT_NOM} + 0.1 V PDO I²C bit is set to 1 after this time has elapsed		10		ms
I_{REV}	Max. reverse current	V_{OUT} forced at V_{OUT_NOM} + 0.1 V after $I_{SINK\_TIME-OUT}$ elapsed		2		mA
T_{SHDN}	Thermal shutdown threshold			150		°C
DT_{SHDN}	Thermal shutdown hysteresis			15		°C

Notes:

(1)In applications where (V_{CC} -V_{OUT}) > 1.3 V the increased power dissipation inside the integrated LDO must be taken into account in the application thermal management design.

(2)Guaranteed by design.

Table 13: Output voltage selection table (data1 register, write mode)

VSEL4	VSEL3	VSEL2	VSEL1	V_{OUT} min.	VOUT pin voltage	V_{OUT} max.	Function
0	0	0	0		0.600		V_{OUT} disabled. The LNBH25LS is set in standby mode
0	0	0	1	12.545	13.000	13.455	
0	0	1	0	12.867	13.333	13.800	
0	0	1	1	13.188	13.667	14.145	
0	1	0	0	13.51	14.000	14.490	
1	0	0	0	17.515	18.150	18.785	
1	0	0	1	17.836	18.483	19.130	
1	0	1	0	18.158	18.817	19.475	
1	0	1	1	18.48	19.150	19.820	

T_J from 0 to 85 °C, V_I = 12 V

Table 14: I²C electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage	SDA, SCL			0.8	V
V_{IH}	High level input voltage	SDA, SCL	2			V
I_{IN}	Input current	SDA, SCL, V_{IN} = 0.4 to 4.5 V	-10		10	µA
V_{OL}	Low level output voltage (1)	SDA (open drain), I_{OL} = 6 mA			0.6	V
F_{MAX}	Maximum clock frequency	SCL	400			kHz

Notes:

(1)Guaranteed by design.

T_J from 0 to 85 °C, V_I = 12 V

Table 15: Address pin characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{ADDR-1}	“0001000(R/W)” address pin voltage range	R/W bit determines the transmission mode: read (R/W=1) write (R/W=0)	0		0.8	V
V_{ADDR-2}	“0001001(R/W)” address pin voltage range	R/W bit determines the transmission mode: read (R/W=1) write (R/W=0)	2		5	V

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 QFN24L (4x4 mm) package information

Figure 12: QFN24L (4x4 mm) package outline

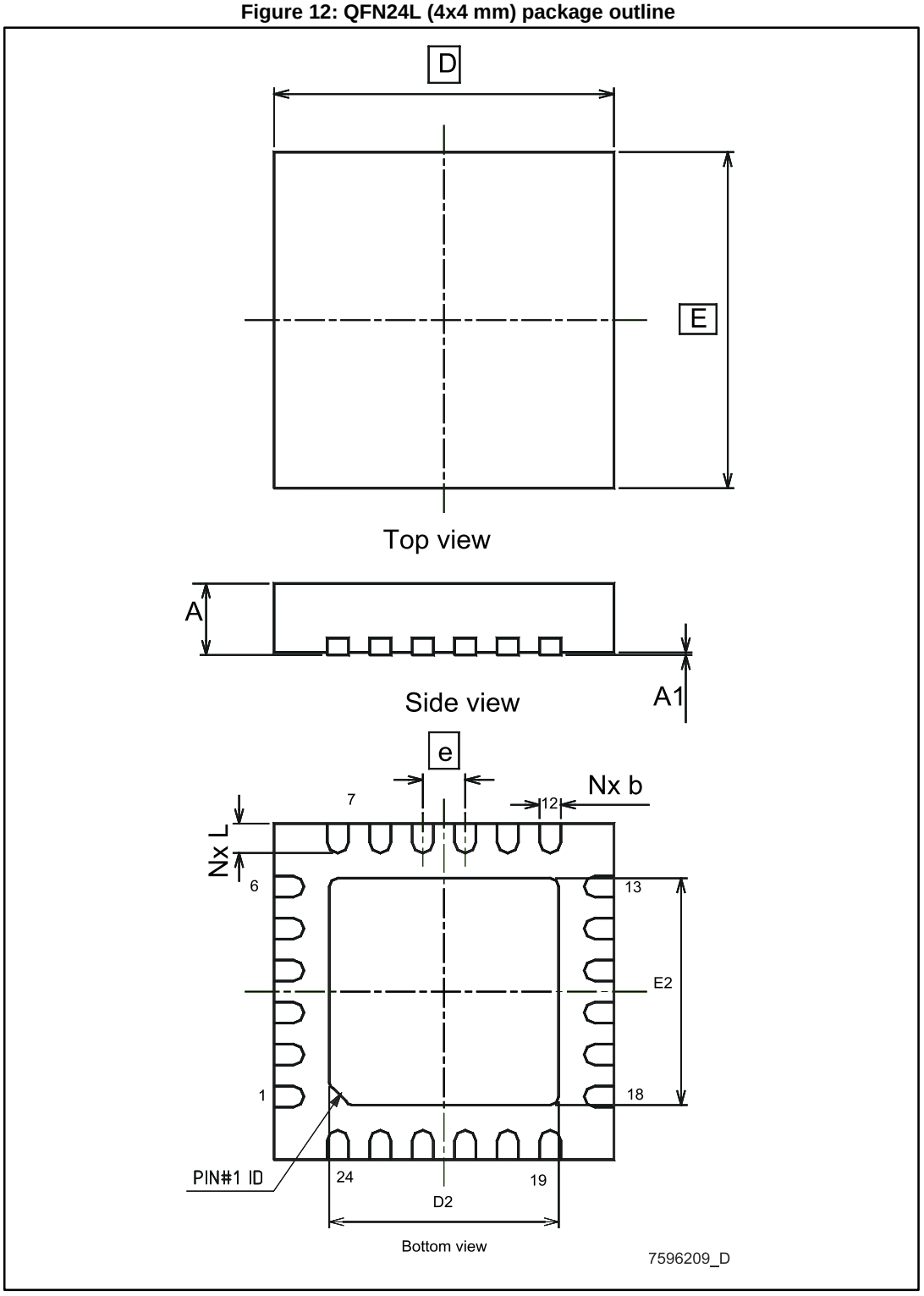
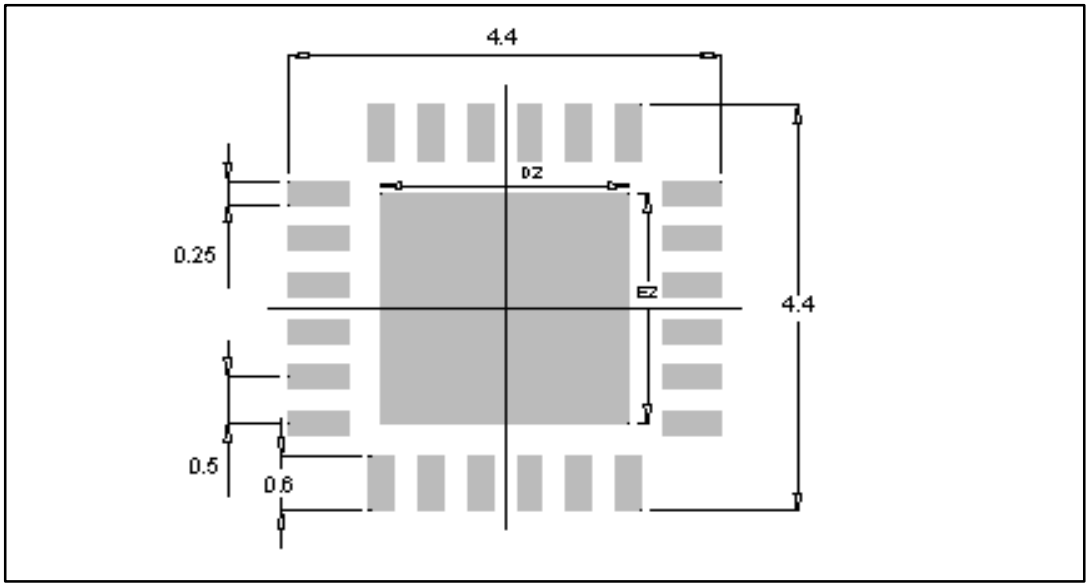


Table 16: QFN24L (4x4 mm) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D	3.90	4.00	4.10
D2	2.55	2.70	2.80
E	3.90	4.00	4.10
E2	2.55	2.70	2.80
e	0.45	0.50	0.55
L	0.25	0.35	0.40

Figure 13: QFN24L (4x4 mm) recommended footprint



10 Revision history

Table 17: Document revision history

Date	Revision	Changes
28-Jul-2014	1	Initial release.
23-Mar-2015	2	Updated table of electrical characteristics.
11-Mar-2016	3	Updated *Figure 10: "Example of writing procedure starting with first data address 0X2"*, *Figure 11: "Example of reading procedure starting with first status address 0X0"*. Updated *Table 12: "Electrical characteristics"* and *Table 13: "Output voltage selection table (data1 register, write mode)"*.

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